APPLICATION

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TITLE: AMPLIFIER WITH VARIABLE SIGNAL GAIN AND MATCHED GAIN BANDWIDTH

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AMPLIFIER WITH VARIABLE SIGNAL GAIN AND MATCHED GAIN BANDWIDTH

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority to U.S. Provisional Application Serial No. 60/285,431 filed on April 19, 2001.

BACKGROUND

[0001] Active pixel sensor (APS) imaging devices are described in U.S. Patent No. 5,471,515. These imaging devices include an array of pixel cells, arranged in rows and columns, that convert light energy into electric signals. Each pixel includes a photodetector and one or more active transistors. The transistors typically provide amplification, readout control and reset control, in addition to producing the electric signal output from the cell.

[0002] The pixels generate analog signals, which are converted into digital signals by analog-to-digital converters (ADCs) for further processing. The analog signal read-out chain may include a gain stage to amplify the analog signals into a range suitable for the ADCs. The magnitude of the gain may range from unity to about eight.

[0003] During readout, the amplifier provides adjustable signal gain with a given amplifier accuracy. The amplifier accuracy determines the required amplifier settling time,

i.e., the interval between the application of the input voltage step and the point at which the output signal reaches and stays within a given error band.

[0004] In many sensors, the unity gain frequency of the amplifier is selected to satisfy the settling time requirement for the worst-case condition, i.e., the maximum signal gain. While this design approach ensures that the amplifier is complying with the settling time requirement at any signal gain selection, it only optimizes the amplifier power consumption in the unique case of the worst-case (maximum) gain setting. For any gain setting lower than the maximum gain setting, the amplifier draws more power than is necessary for the required settling time.

SUMMARY

[0005] A sensor includes a pixel array, a read-out stage, and a gain stage that includes a differential amplifier with an adjustable gain. The differential amplifier may change its gain in response to the magnitude of a signal readout from the pixel array. The differential amplifier includes an input transistor with an adjustable transconductance. The transconductance of the input transistor is proportional to the power consumption of the

input transistor. The input transistor includes two or more sets or parallel transistors, each set connected to a different bias current supply. A transconductance controller can change the bias currents supplied to one or more sets of parallel transistors and consequently change the transconductance, and power consumption, of the input transistor. The transconductance controller can select a transconductance setting that is associated with a selected gain setting in order to more efficiently match the power consumption of the amplifier to its gain.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 is a block diagram of a sensor according to an embodiment.

[0007] Figure 2 is a schematic diagram of a differential amplifier with variable gain according to an embodiment.

[0008] Figure 3 is a schematic diagram of the differential amplifier of Figure 2 in greater detail.

[0009] Figure 4 is a block diagram of a bias current selection and generation circuit according to an embodiment.

[0010] Figure 5 is a schematic diagram of a current multiplexer according to an embodiment.

[0011] Figure 6 is a flowchart describing an operation for matching a current bias to a selected gain value according to an embodiment.

DETAILED DESCRIPTION

[0012] A sensor 100 according to an embodiment includes a pixel array 102. The sensor 100 may be an active pixel sensor (APS), in which the pixel array includes a grid of individually addressable pixels 104 arranged in rows and columns. Each pixel 104 includes a photodetector, such as a photogate, photodiode, or pinned photodiode. The photodetector converts light energy received in the form of photons into an electric charge. This electric charge corresponds to an amount of light that the pixel 104 receives during an exposure to an image. The amount of light received by each pixel in the array during exposure to the image is used by the sensor 100 to produce a signal indicating a corresponding digital image.

[0013] After the exposure and a subsequent integration period, the pixel array 102 is read out row-by-row for processing. The electric charge held in the pixel in each column in the selected row is output to a sample-and-hold (S/H) unit 110 in a S/H block 112. The S/H unit 110 may

include a sampling switch and a holding capacitor to store the sampled analog signal.

[0014] The sampled analog signals are passed from the S/H block 112 to a gain stage 120 before being sent to analog-to-digital converters (ADCs) in an ADC block 130 for conversion to digital signals. The ADCs may have a range of analog signals they can convert into discrete digital values. The analog signals generated by pixels exposed to very low levels of light may fall below the lower limit of this range. The gain stage 120 selects an appropriate gain setting to amplify such small analog signals to values that are within a suitable range for the ADCs. The gain stage 120 may have, for example, a minimum gain setting of 1 and a maximum gain setting of 8.

[0015] The gain stage 120 may include a class A differential amplifier 200 with variable gain, as shown in Figure 2. The differential amplifier 200 has two input nodes 202, 204. The input voltages Vin_n and Vin_p applied to these nodes are equal in amplitude and 180° out of phase. The differential amplifier also has two output nodes 206, 208. The output voltages $Vout_n$ and $Vout_p$ are equal in amplitude and 180° out of phase.

[0016] The gain provided by the differential amplifier 200 may be adjusted by selecting an input capacitance and a

feedback capacitance. The input capacitance may be set by selectively opening and closing switches sw_0 - sw_5, and the feedback capacitance may be set by selectively opening and closing switches sw_6 - sw_7. Each switch sw_0 - sw_7 is coupled to an associated capacitor C_0 - C_7. Exemplary values for C_0 - C_7 are 12.5 fF, 25 fF, 50 fF, 100 fF, 200 Ff, 400 fF, 100 fF, and 100 fF, respectively. The ratio of the input capacitance to the output capacitance determines the gain setting.

[0017] The power consumed by the amplifier increases with its gain bandwidth (GBW). The GBW of the amplifier is proportional to the transconductance (g_m) of the input transistors in the amplifier, and is given by $\frac{gm}{2\pi C}$, where C is the load capacitance. Since the transconductance is proportional to the bias current of the input transistor, the GBW may be varied by changing the bias current of the input transistor.

[0018] Figure 3 illustrates a differential amplifier 300 with variable gain and a variable GBW, which may be selected in response to the selected gain in order to increase the efficiency of the amplifier. Rather than having two input transistors for Vin_n and Vin_p, respectively, the input transistors are segmented into two

sets of input transistors 302, 304 and 312, 314. Each set of transistors is connected in parallel. The bias current through the set of parallel transistors 302, 304 is controlled by bias transistor 320 with input terminal $tail_1$. The bias current through the set of parallel transistors 312, 314 is controlled by bias transistor 322 with input terminal $tail_2$.

[0019] The total bias current input to the differential amplifier 300 is $2Ib_1 + 2Ib_2$. The bias transistors 320, 322 form current mirrors. Each bias transistor controls the bias current through the two parallel transistors to which it is connected. The $tail_1$ bias transistor 320 sets the portion of the bias current flowing through each of the parallel transistors 302, 304 to Ib_1, and the $tail_2$ bias transistor 322 sets the portion of the bias current flowing through each of the parallel transistors 312, 314 to Ib_2.

[0020] The input transconductance, g_m, and hence the GBW and power consumption, of the amplifier may be varied by varying the bias current through one or both sets of parallel transistors (Ib_1 and/or Ib_2). In an embodiment, the bias current applied to terminal $tail_2$ is reduced for lower gain settings. When the bias current Ib_2 gets close to the operating threshold for the parallel transistors 312, 314, i.e., the current at which the transistors begin

to turn off, the bias current applied to terminal $tail_1$ may then be reduced to further lower the transconductance at the input of the differential amplifier 300.

[0021] As shown in Figure 4, a gain decoder 402 selects a bias current setting in response to the gain setting. The gain decoder 402 controls two current multiplexers 410, 420. Each current multiplexer may include an array of ten 1 μA current sources 500-509, as shown in Figure 5. Each current source 500-509 may be selected by closing a corresponding control switch s<0> - s<9>. The total current output by a current multiplexer depends on the number of control switches selected by the gain decoder 402.

[0022] The currents 415, 425 output from the current multiplexers 410, 420 are input to a bias generator 430. The bias generator 430 uses these currents to generate bias voltages in response to the selected gain setting and applies the bias voltages to terminals 350-355 (for $bias_1$, $bias_2$, $bias_3$, $bias_4$, $tail_1$, and $tail_2$, respectively). Figure 6 is a schematic diagram of a bias generator circuit 600 according to an embodiment.

[0023] In an embodiment, the differential amplifier 300 may have three bias current settings; HIGH, MED, and LOW. The gain decoder 402 may decode these three settings from

the states of switches sw_3-sw_6. A HIGH setting corresponds to a gain between 6 and 8, a MED setting corresponds to a gain between 3 and 6, and a LOW setting corresponds to a gain between 1 and 3. For the HIGH setting, all switches for both current multiplexers 410, 420 are closed, providing 100% of the available bias current. For the MED setting, all switches in the current multiplexer 410 are closed, and switches s<0> and s<1> are closed in the current multiplexer 420, providing 60% of the available bias current. For the LOW setting, switches s<0> to s<3> are closed in the current multiplexer 410, and all switches are open in the current multiplexer 420, providing 20% of the available bias current.

[0024] Figure 6 illustrates a flowchart describing a bias selection and generation operation 600 according to an embodiment. The flow of the operation 600 is exemplary, and blocks in the flowchart may be skipped or performed in different order according to alternate embodiments.

[0025] A gain setting is selected (block 602) in response to the amplitude of the analog signal output from a pixel in a selected row. The switches sw_0-sw_7 are selectively opened and closed to produce the selected the gain setting (block 604). For example, in the present embodiment, a gain of 1 is produced when all switches but

switch sw_7 are open, a gain of about 4 is produced when all switches are closed, and a gain of about 8 is produces when all switches but sw_6 are closed.

[0026] The gain decoder determines the bias current setting (HIGH, MED, or LOW) from the state of switches sw_3 - sw_6 (block 606). The gain decoder controls the current multiplexers 410, 420 to generate the current appropriate for the gain setting and input the currents to the bias generator (block 608). The bias generator generates the appropriate bias voltages for terminals 350-355 ($bias_1$, $bias_2$, $bias_3$, $bias_4$, $tail_1$, and $tail_2$) (block 610) and sets the bias current in the bias transistors 320, 322 appropriate for the gain setting (block 612).

[0027] In alternate embodiments, the input transistors may be split into more than two sets of parallel input transistors, each with an associated bias transistor. This may provide more precise tuning of the bias current to the various gain settings. Each gain setting may be associated with a distinct bias current setting to optimize power consumption in the amplifier for that gain setting.

[0028] With more sets of parallel input transistors, the bias current may be reduced in one set until the input transistors in that set begin to turn off, at which point the bias current in another set may be reduced. The use of

multiple sets of parallel input transistors may enable greater tuning of the bias current settings to the various gain settings.

[0029] It may be desirable to provide a minimum amount of bias current through all input transistors to prevent the input transistors from turning completely OFF, which may produce unpredictable behavior in the amplifier.

[0030] An advantage of matching the GBW to a selected signal gain may be reduced power consumption of the amplifier. Another advantage may be reduced root mean square (RMS) voltage noise at the output of the amplifier. The total RMS voltage noise at the output of the amplifier may be proportional to the root square of the amplifier's GBW. For a selected signal gain, matching the GBW to the signal gain selects the lowest GBW value for a given settling time requirement. This may produce less noise at the amplifier output compared to an amplifier that is designed for the worst-case gain setting (i.e., with no GBW matching to the selected signal gain).

[0031] A number of embodiments have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. Accordingly, other embodiments are within the scope of the following claims.